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Design Guidelines – May 2013

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Introduction

These Guidelines set out best practice to reduce the cost of your boards and to minimize the risk of errors arising during manufacture. Not all possible PCB design features are available on all our services. Look at our services overview to see more details. On some specific features we highlight the availability in a particular service.

The world is divided into a part that works with the Metric system and a part that works with the Imperial system for defining measurements. The "µm" is 25.4 times smaller than the "Mil". Dimensions for electronics are driven smaller all the time. To ensure the highest quality possible, we decided many years ago to work exclusively in the Metric system in our front end department. Therefore the basis of all measurements given in this document and in our website is the Metric system. All Imperial values are there for clarification and general understanding only.

There is no general consensus throughout the global PCB industry on terminology, so if we feel any term we use may be unclear we have tried to explain it when it first appears.



Input data formats

Accepted data formats for PCB layout data are:

Artwork:

- Gerber RS-274X (Extended Gerber with embedded apertures - developed by Gerber Systems)
- DPF (Dynamic Process Format - developed by Ucamco NV)
- Gerber RS-274D (Standard Gerber with a separate aperture file - developed by Gerber Systems)
- Eagle .BRD file (CAD-data from CADsoft now Farnell)

Artwork means all copper layers, soldermask and legend layers, board outline or mechanical layer, SMD paste layers, carbon layers, peel-off layers, etc.

Drilling:

- Excellon (1 or 2) + appropriate tool list (ideally embedded)
- Sieb&Meyer + appropriate tool list (ideally embedded)
- Gerber format RS-274X or RS-274D (only true drill data, not a drill map)
- DPF (only true drill data, not a drill map)

IMPORTANT:

Please supply **ONLY ASCII**-encoded files. These files are man-readable so that our engineers can check them visually if needed during data preparation. So we don't accept formats such as EIA or EBCDIC.

CAD PCB design data, other than from EAGLE, is NOT ACCEPTED!

We **do not accept CAD PCB design data other than EAGLE.**

1. Converting CAD data into production data may lead to errors which we cannot cross-check
2. It is impossible to have legal copies of every CAD PCB design package in the market and to have the necessary knowledge to use them all correctly. As designers do not all use the same software version, we would need to have a whole range of update patches as well.

Gerber is clear and unambiguous. It has been the industry-standard format for PCB manufacture for many years. Every PCB design package can output Gerber data and the process will be fully described in your CAD PCB design package handbook or help-files.

You can check the accuracy of the Gerber output data by downloading one of the many free Gerber viewers available on the internet. We recommend GC-Prevue available as freeware from www.graphicode.com.

Input data requirements

1. **Preferred** data formats are:
 - For Artwork -- Extended Gerber (RS-274X)
 - For Drilling -- Excellon1 + appropriate tool list (ideally embedded)

PCB Visualizer: For reasons of automated analysis and visualisation, the PCB Visualizer only accepts Extended Gerbers (RS-274X) or an EAGLE .BRD file.

2. **Provide us ONLY** with the data files needed for production. These are:
 - Gerber files for the copper layers, soldermask and legend layers, mechanical layer and SMD paste layers. Plus carbon, peel-off and via-fill layers as needed.
 - Excellon drill file(s) for drilling.
 - If you want us to prepare a customer panel ("array", "matrix" or "biscuit") from the single board data to your individual specification, the panel plan can be supplied as a Gerber or DPF file.

Please DO NOT provide any additional files such as original CAD data (other than Eagle), Graphiccode GWK files, PDF files, Word files (doc), Excel files (xls), part lists, placement and assembly information, etc.

Where possible check your generated output data (Gerber & Excellon files) either using PCB Visualizer or with a Gerber viewer before you send it on to production. Make sure that all instructions or other necessary input needed for making the boards are included in the Gerber and Excellon files.

3. Use clear and easy to understand file naming and try to avoid long filenames. Make sure that we can easily determine the layer function from the filename.

Good file naming:

Name	Size	Type
SMALLTCSV2BALE.BOT		
SMALLTCSV2BALE.SMB	141101-A_SOLDERMASK BOTTOM.GBR	3 KB GBR File
SMALLTCSV2BALE.SMT	141101-A_SILKSCREEN TOP.GBR	10 KB GBR File
SMALLTCSV2BALE.TOP	141101-A_SILKSCREEN BOTTOM.GBR	2 KB GBR File
SMALLTCSV2BALE.DRD	141101-A_SIGNAL TOP.GBR	3 KB GBR File
SMALLTCSV2BALE.SST	141101-A_SIGNAL BOTTOM.GBR	10 KB GBR File
SMALLTCSV2BALE.DTS	141101-A_DRILL PROGRAM.GBR	3 KB GBR File
	141101-A_SOLDERMASK TOP.GBR	3 KB GBR File

File naming is too long, not advisable:

Name	Size	Type
cam_unit_lamp_led_guide-Master Design(Stencil top).gbr	1 KB	GBR File
cam_unit_lamp_led_guide-Master Design(solder mask top).gbr	2 KB	GBR File
cam_unit_lamp_led_guide-Master Design(solder mask bottom).gbr	6 KB	GBR File
cam_unit_lamp_led_guide-Master Design(Silkscreen Top).gbr	210 KB	GBR File
cam_unit_lamp_led_guide-Master Design(silkscreen bottom).gbr	14 KB	GBR File
cam_unit_lamp_led_guide-Master Design(drills plated).drl	1 KB	DRL File
cam_unit_lamp_led_guide-Master Design(drill unplated).drl	3 KB	DRL File
cam_unit_lamp_led_guide-Master Design(Bottom).gbr	10 KB	GBR File
cam_unit_lamp_led_guide(CAMPlot).txt	9 KB	Text Document
cam_unit_lamp_led_guide-Master Design(Top).gbr	5 KB	GBR File

Bad file naming: no info on layer function in the file names:

Name	Size	Type
filter_v1_0.inf	4 KB	Setup Information
Layer_1.gbr	filter_v1_0.gb4	3 KB GB4 File
Layer_3.gbr	filter_v1_0.gb3	2 KB GB3 File
Layer_4.gbr	filter_v1_0.gb2	10 KB GB2 File
Layer_5.gbr	filter_v1_0.gb1	5 KB GB1 File
Layer_6.gbr	filter_v1_0.gb0	1 KB GB0 File
Layer_7.gbr	filter_v1_0.drl	2 KB DRL File

4. **DO NOT scale** your data. All data provided must be scale 1/1 (100%).
5. Make sure that your Gerber files DO NOT contain apertures with a zero-size (size = 0.00mm or inches) and that your Excellon data DOES NOT have zero-sized tools (size=0.00mm or inches).

6. Use the same offset for all your Gerber layers and the Excellon drill data. Preferably use no offset at all.



7. Use the same units (mm or inch) in your Gerber & Excellon output files as in your CAD PCB design software. This will eliminate conversion or rounding errors.
8. Use the same resolution (grid) for your Gerber & Excellon data to allow a perfect match.

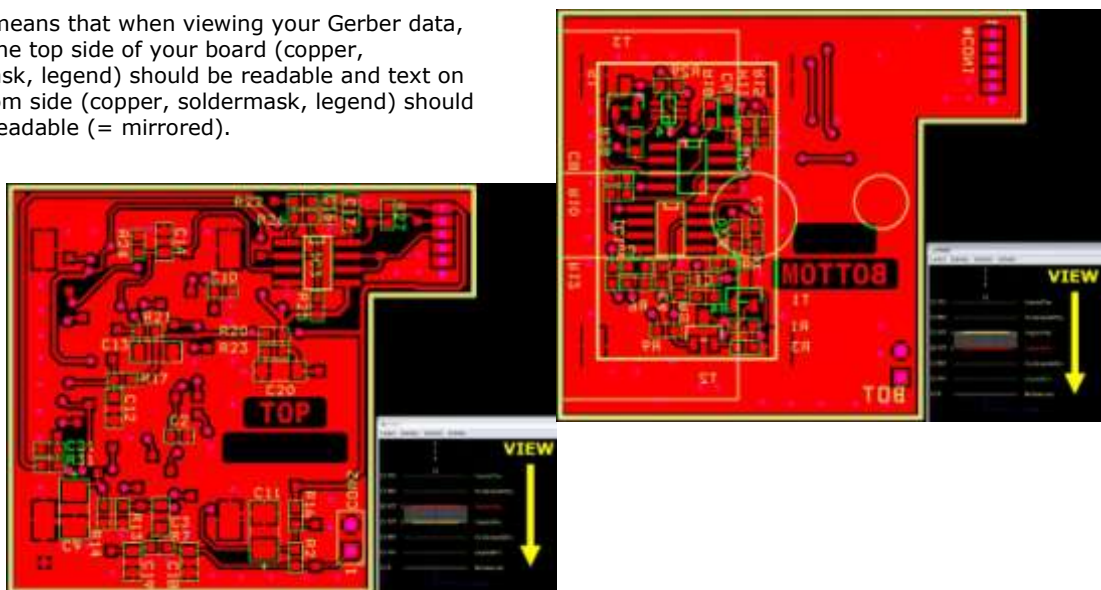
Also make sure that the resolution (grid) used for your output (Gerber & Excellon) is at least a factor 10 better than the resolution (grid) used in your CAD PCB design software.

Example: If you use a 10 mil resolution to draw your board in your CAD PCB design software, then use a 1mil output resolution for your Gerber & Excellon output.

9. Make sure that your data is supplied as **seen from top to bottom through the PCB. DO NOT mirror** (or reflect) any data layer – image or drill.

Viewing a PCB from top to bottom through the board is the universal practice in the PCB industry. We view and handle your data in that way, as does your CAD PCB design software.

-> This means that when viewing your Gerber data, text on the top side of your board (copper, soldermask, legend) should be readable and text on the bottom side (copper, soldermask, legend) should be non-readable (= mirrored).



10. Put some small text (board identification, company name, etc...) in the copper layers. Make sure the text complies with the readability rules. This will help us to avoid mirroring errors.
11. RECOMMENDATION. In your Gerber files use flashed pads as often as possible.
12. RECOMMENDATION. In your CAD PCB design software try to create an aperture list for Gerber output which only shows the apertures used in the design.
13. Make sure that you include the board outline on all layers. This will enable us to properly align all layers in case of an offset problem. Also include the board outline in a separate Gerber mechanical plan.

Classification

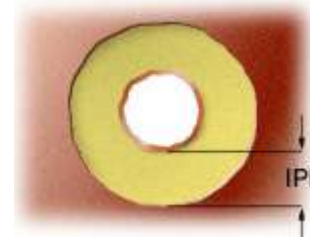
Introduction

We use "pattern classes" and "drill classes" as convenient shorthand to measure the manufacturability of the PCB. This controls whether the board can be pooled or not and has an impact on the pricing.

The pattern class covers

- The minimum sizes for copper track (conductor) and gap (isolation) for Outer and Inner layers:
 - Outer layers OTT = Track to Track , OTP = Track to Pad, OPP = Pad to Pad and OTW = Track Width
 - Inner layers ITT = Track to Track , ITP = Track to Pad, IPP = Pad to Pad and ITW = Track Width
- The minimum copper rings on outer and inner layers (OAR = Outer Annular Ring, IAR = Inner Annular Ring)
- The minimum IPI (Inner layer Pad Isolation):
IPI is the clearance between the edge of any unconnected hole (plated or non-plated) and the nearest copper (plane, track, pad). This is measured from the production tool size.

Minimum IPI value is always $IAR + 75\mu\text{m}$ (3mil)



The smallest of these values determines the pattern class.

The drill class is based on the smallest production tool size on the board.

For more information **see the current Classification table on the next page**

IMPORTANT: Annular Ring calculations are done from the production TOOLSIZE for the holes, not from the finished hole ENDSIZE. --> For the conversion rules for ENDSIZE to TOOLSIZE see Holes section 6.

1. The Classification table shows the lower limit values of any given class.
2. The Annular Ring values OAR and IAR in the classification table are for plated holes (PTH). For connected non-plated (NPTH) holes we recommend a minimum annular ring of 0.30mm (12mil). As NPTH holes have no plated barrel, a smaller annular ring may lift during soldering or break away even during normal operating conditions.
3. The thickness of the starting copper foil determines the minimum pattern values that are possible. This means that the highest pattern class possible depends on the copper thicknesses. Thicker copper needs a wider isolation for reliable etching – see the Classification table.

Not all copper thicknesses are available in all services. See our services overview document for guidance.

4. RECOMMENDATION. Do not design up to the limits of any given classification. Always keep a small margin above the classification limits. This may be needed where the CAD output does not exactly match the design data due to rounding or matching errors caused by different units or grids (see section Input data requirements points 7 & 8)

Eurocircuits - PCB design classification overview

Pattern Class	class 3		class 4		class 5		class 6		class 7		class 8		class 9		class 10	
	P+S+R+I	P+S+R+I	P+S+R+I	P+S+R+I	P+S+R+I	P+S+R+I	P+S+R+I	P+S+R+I	S+R	S+R	S+R	S+R	S+R	S+R	S+R	S+R
Service	0.250	10	0.200	8	0.175	7	0.150	6	0.125	5	0.100	4	0.090	3.5	<0.090	<3.5
OTT-OTP-OPP	0.250	10	0.200	8	0.175	7	0.150	6	0.125	5	0.100	4	0.090	3.5	<0.090	<3.5
OAR	0.200	8	0.150	6	0.150	6	0.125	5	0.125	5	0.100	4	0.100	4	<0.100	<4
ITW	0.250	10	0.200	8	0.175	7	0.150	6	0.125	5	0.100	4	0.090	3.5	<0.090	<3.5
ITT-ITP-IPP	0.250	10	0.200	8	0.175	7	0.150	6	0.125	5	0.100	4	0.090	3.5	<0.090	<3.5
IAR	0.200	8	0.150	6	0.150	6	0.125	5	0.125	5	0.125	5	0.125	5	<0.125	<5
IPI	0.275	11	0.225	9	0.225	9	0.200	8	0.200	8	0.200	8	0.200	8	<0.200	<8

The smallest value (OTW, OTT-OTP-OPP, OAR, ITW, ITT-ITP-IPP, IAR, IPI) determines the **Pattern Class** of the board

Base Cu min Pattern values

Base Cu OL	OTT-OTP-OPP		OTW	
	min	max	min	max
12µm	0.090	3.5	0.090	3.5
18µm	0.125	5	0.090	3.5
35µm	0.175	7	0.125	5
70µm	0.250	10	0.200	8
105µm	0.300	12	0.250	10

Base Cu IL	ITT-ITP-IPP		ITW	
	min	max	min	max
12µm	0.090	3.5	0.090	3.5
18µm	0.100	4	0.090	3.5
35µm	0.125	5	0.125	5
70µm	0.250	10	0.200	8
105µm	0.300	12	0.250	10

Smallest PHD : Production Hole Diameter or tool size = finished hole size + 0.10mm/4mil for Plated Through Holes + 0.00mm/0mil for Non Plated Through Holes

Drill Class	class A		class B		class C		class D		class E		class F	
	P+S+R+I	P+S+R	P+S+R	P+S+R	P+S+R	P+S+R	S+R	S+R	S+R	S+R	S+R	S+R
Service	0.60	0.026	0.45	0.018	0.35	0.014	0.25	0.010	0.20	0.008	<0.20	<0.008
min PHD												
PTH	0.50	0.022	0.35	0.014	0.25	0.010	0.15	0.006	0.10	0.004	<0.10	<0.004
NPTH	0.60	0.026	0.45	0.018	0.35	0.014	0.25	0.010	0.20	0.008	<0.20	<0.008

Corresponding finished holes sizes

The smallest value (PHD) determines the **Drill Class** of the PCB

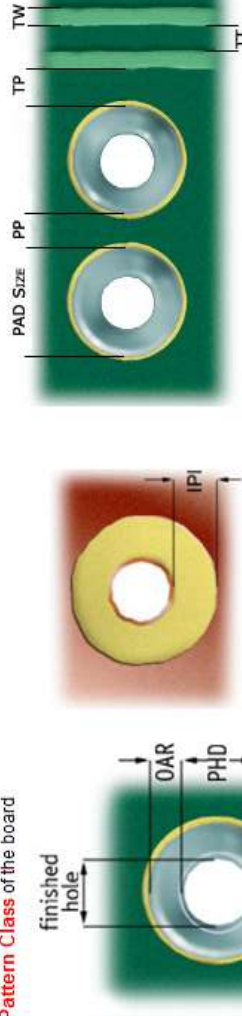
Max. PCB thickness to Drill Class	3.20	0.125	3.20	0.125	2.40	0.093	2.00	0.079	1.60	0.062	mm-inch	Aspect ratio is 1 / 8
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Note A: VIA holes are Plated Through Holes, default defined as <=0.45mm (18mil) for all services or <= as defined by the customer in the order details.

Note B: VIA holes have a maximum negative tolerance of 0.30mm (12mil)

This classification table can only be put into praxis on PCB designs that have a Plating Index of 0.40 or higher. This is calculated in the PCB Visualizer analysis and displayed in the PCB Visualizer order details.

Services Index : P = PCB proto S = STANDARD pool R = RF pool I = IMS pool



Preceding letters O and I stand for Outer- and Inner layer
Example: OTW = Outer layer Track Width

OAR : smallest OAR (Outer layer Annular Ring = 1/2 (Outer layer pad diameter - PHD))

IAR : smallest IAR (Inner layer Annular Ring = 1/2 (Inner layer pad diameter - PHD))

IPI (Inner layer Pad Insulation) : Clearance between edge PTH and any nearest copper



Holes

1. Tool lists for drill files are **ALWAYS** read by our CAM systems as finished hole sizes (ENDSIZE).
2. All PCB drills are manufactured in increments of 0.05 mm. So we convert the drill sizes given in the drill files or tool lists into millimeters and round to the nearest 0.05mm.

For example:

- Drill size of 31mil is converted to 0.7874mm and then rounded to 0.80mm.
- Drill size of 32mil is converted to 0.8128mm and then rounded to 0.80mm.
- Drill size of 33mil is converted to 0.8382mm and then rounded to 0.85mm.

3. If possible, provide separate drill files for plated (PTH) and non-plated (NPTH) holes. If this is not possible, always specify different tools for PTH and NPTH holes and mark clearly which tools are PTH and which tools are NPTH.
4. When no PTH/NPTH info is given we use the following rules to determine PTH/NPTH:

For 0-layer and 1-layer boards: → ALL holes are considered as NPTH by default.

For 2-layer and multilayer boards: → ALL holes are considered PTH except the following cases which are considered NPTH:

- Non-connected holes without copper pads.
- Non-connected holes where the copper pad size is equal to or smaller than the drill TOOLSIZE (the copper pad will be removed in single image preparation)
- Connected holes with a copper pad on 1 side (outer), no connection on any other layer (outer or inner) and no copper pad on the other side (outer).

5. VIA holes are Plated Through Holes, defined by default as $\leq 0.45\text{mm}$ (18mil). VIA holes have a maximum negative tolerance of 0.30mm (12mil) and may be reduce to accommodate a larger annular ring when needed. If you need component holes of 0.45 mm or smaller with standard component hole tolerances, you can specify this in the order details.

IMPORTANT:

This default via-rule affects:

- Finished hole size to production drill size (ENDSIZE to TOOLSIZE) conversion
- The standard tolerance on via hole ENDSIZE diameter.

6. To allow for the plating in the hole we drill holes prior to plating at a larger size (drill over-sizing) The conversion rules from finished hole ENDSIZE to production TOOLSIZE are:
 $\text{TOOLSIZE} = \text{ENDSIZE} + 0.10\text{mm}$ (4mil) for Plated Through Holes (PTH)
 $+ 0.00\text{mm}$ (2mil) for Non Plated Through Holes (NPTH)
7. Standard tolerances on drill ENDSIZE diameter.

NPTH holes	+/- 0.05mm (+/- 2mil)
PTH holes	+/- 0.10mm (+/- 4mil)

VIA holes have a maximum negative tolerance of 0.30mm (12mil). For definition of VIA holes see point5 above.

When no tolerances are specified in your data, we will produce according to our standard tolerance specifications.

If you require tighter tolerances these should be clearly indicated in the mechanical layer and tool list. They will increase the cost of the PCB so should not be used without a compelling reason.

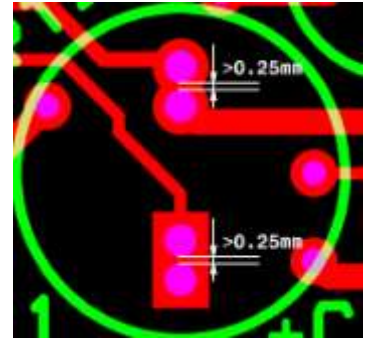
8. Drilled holes that overlap the board contour can be:
 - NPTH holes without copper pads: these NPTH holes will be treated as part of the board outline.
 - PTH holes with copper pads: these will be taken as "plated holes on the board edge" or "Contour Cut PTH drills" and should be clearly indicated in the mechanical layer.

REMARK: Plated holes cutting the board edge are not available in the **PCB proto** service.

9. Overlapping drill holes.

Do not overlap drill holes. These can cause broken drill bits and the small pieces of material left behind may cause voids in the plated hole barrels. The minimum drill hole to drill hole distance is 0.25mm (10mil). This is measured edge to edge of the drill TOOLSIZE.

Do not use overlapping drill holes to define slots. See section Mechanical Layer for the correct way to indicate slots and internal cut-outs.



10. Annular Rings on oblong pads.

The rules for annular rings on oblong pads are **NOT** different from round pads, but we allow some exceptions to the rules.

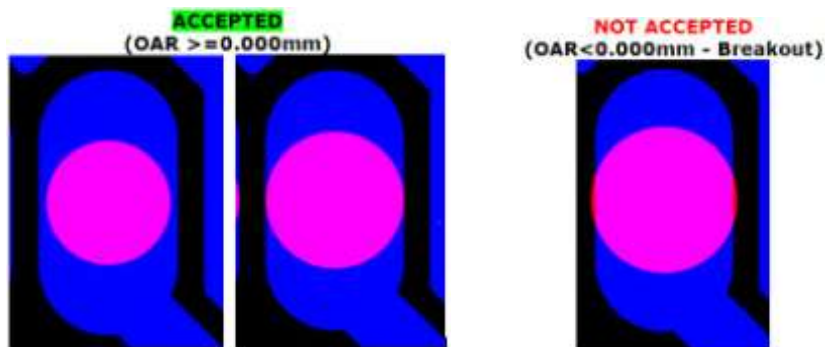
Oblong pads with NPTH holes:

- MUST ALWAYS FULLY COMPLY with the standard Annular Ring rules for any given pattern class.
- The recommended Annular Ring for any NPTH hole is 0.30mm (12mil) - see section Classification – point 2

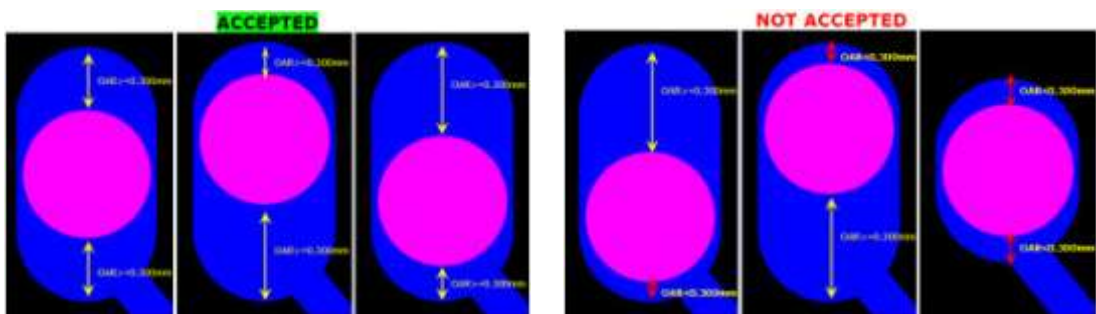
Oblong pads with PTH holes

The measurements below are taken from the production TOOLSIZE.

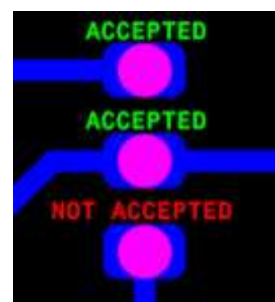
- On the **smallest side** of the oblong pad the **OAR must be $\geq 0.00\text{mm}$ (0mil)** (i.e. no breakout is allowed)



- On the **longest side** of the oblong pad **in both directions** the **OAR must be $\geq 0.300\text{mm}$ (12mil)** (but the hole need not be in the centre of the pad)



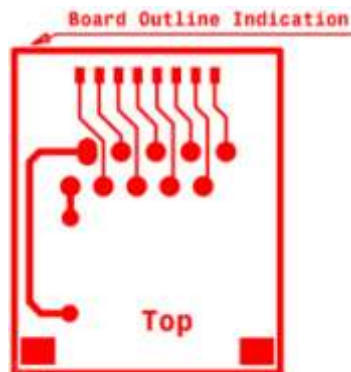
The hole may not be positioned in such a way that it could disconnect the pad from the track..



Copper layers

1. When generating output, use “flashes” for pads and avoid “painted” pads (i.e. pads filled with small draws)
2. Avoid filling large copper areas or copper planes with small draws (“painting”). Where possible, use contours or polygons to construct areas or planes. Contourized areas or Polygon Area fill are standard features in Extended Gerber output (RS-274X).
3. When generating output include the board outline in your copper layers.

This is best done using a small line - e.g. 0.50mm (20mil) wide - where the center of the line is the exact board outline. We will remove this line during the making of the production tools.



4. Remove copper pads from NPTH holes if these pads are not used or connected to other copper. If you require copper pads on NPTH holes then it is advisable to use a minimum Outer Annular Ring (OAR) of 0.30mm (12mil) - see Classification point 2.
5. Check your final design for small areas of unconnected copper or narrow copper webs and slivers which can lead to problems in production.



X: Must meet classification criterion for minimum Track Width (TW).

A: Avoid if possible.

B: Preferred design

6. Minimal clearance between edge of board and pattern.

For routed boards:

- 0.25mm (10mil) on outer layers
- 0.40mm (16mil) on inner layers

For boards with scoring (V-cut):

- 0.45mm (18mil) on outer and inner layers

7. If you require a copper area or plane to extend up to the board edge, then clearly indicate this in the mechanical layer.

Copper up to the board edge should only be used where absolutely necessary because:

1. There is a risk of a rough board edge as the copper may tear during contour routing (profiling).
2. The copper can create electrical shorts between layers.
3. Copper up to the board edge is NOT compatible with scoring (V-cut).

8. If you require the board edge or part of it to be plated, then clearly indicate this in the mechanical layer.

9. Any text placed in a copper layer has to comply with the design rules for the given class (see classification table).

All copper text must be correctly readable. As a **PCB is always viewed from top to bottom through the PCB**, text on the top layer of your board should be readable and text on the bottom layer should be non-readable or mirrored.

10. Avoid “peelables”.

“Peelables” occur during production and are small/narrow pieces of photo resist enclosed by pads, traces and/or planes which may “peel” away during processing and cause short or open circuits. All copper even within the same net must comply with the design rules for the given class (see classification table).



11. For gold connectors do not place any plated holes (PTH), SMD or other pads closer than 2.00mm (80mil) to the gold fingers – see drawing.



12. ALWAYS provide the proper layer sequence for a multilayer board.

The layer sequence can be given in several ways:

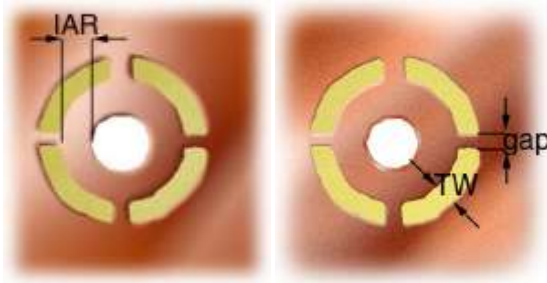
- Indicate the layer numbers in the copper image by placing a logical number in each layer (1 for top layer, 2 for inner1, 3 for inner2, etc....). Make sure the numbers are positioned in such a way that they do not overlap, and can be seen through the complete PCB.



- Name each layer file in a way which indicates clearly the sequence to be used (e.g. T(op), I(nner)1, I(nner)2, B(ottom)).
- Include in your Gerber mechanical layer a clear build-up drawing including all copper layers, soldermask and legend layers, additional layers like peel-off or carbon in the correct sequence and with the correct corresponding data file name.
- Include a simple ASCII text file with your data indicating which file is to be used for which layer, preferably already in the correct build-up sequence (this is the least preferred solution: it is better if the build-up is indicated in the Gerber data as in the previous 3 suggestions).

13. RECOMMENDATION. If holes on inner layers are not connected on a particular layer, do not give them a pad in the inner layers. In any case we will remove all unconnected pads on the inner layers.

14. Thermal definition: make sure your thermal relief pads are properly defined and comply with the chosen pattern classification for Annular Rings (AR), Track Widths (Thermal Segment Width) and Gaps.

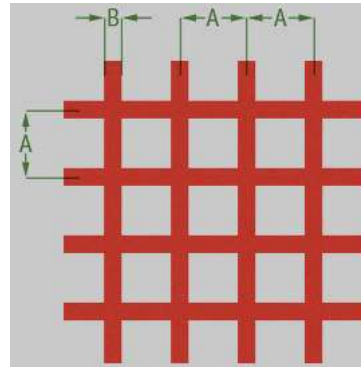


Good practice for Thermals is to work with a Gap of 0.20mm (8mil) and a Thermal Segment Width of 0.20mm (8mil).

15. Hatching patterns. RECOMMENDATION: use full copper rather than hatching patterns in copper planes.

If you need a hatching pattern, then use following minimum settings:

- Minimum distance center to center between tracks of pattern (**A**): 0.60mm (24mil)
- Minimum track width for pattern (**B**): 0.20mm (8mil)



IMPORTANT:

Any hatching pattern that **DOES NOT meet** these minimum requirements will be converted into a full copper plane.

BGAs

Designers sometimes ask us for some guidelines on BGAs. Independent of particular components you need to consider what size of pads you need to use and how many connections you need to bring out of the package. You should compare this with our current Classification table.

Using only poolable options, you need to bear in mind that the minimum track to track and track to pad isolation is 0.100mm (4mil), the minimum track width is 0.100mm (4mil) and the smallest finished hole size is 0.15mm (6mil) if you want vias under the device. For a 0.15mm (6mil) finished hole size the smallest pad we need for a good annular ring is 0.450mm (18mil) on outer layers and 0.500mm (20mil) on inner layers.

Making your board non-poolable, you can reduce the minimum track width and isolation to 0.090mm (3.5mil), the minimum hole size to 0.10mm (4mil) with a minimum pad size of 0.400mm (16mil) on outer layers and 0.450mm (18mil) on inner layers. This will increase the price.

Mechanical layer

1. RECOMMENDATION: ALWAYS include a Gerber mechanical layer in your data set.

IMPORTANT:

- A proper mechanical layer is **VITAL to a good and flawless production** of the PCB as it should provide us with all the needed mechanical information for the construction of your PCB.
- In case of **cut-outs or slots** in your PCB, this layer is essential to the production!
- **DO NOT scale** your mechanical layer, it should be 1 to 1 and reflect the exact dimensions of the PCB.
- The mechanical layer is – as for all layers - also **viewed from top to bottom through your PCB**, so do not mirror the mechanical layer.
- **ONLY** include information in your mechanical layer that is needed

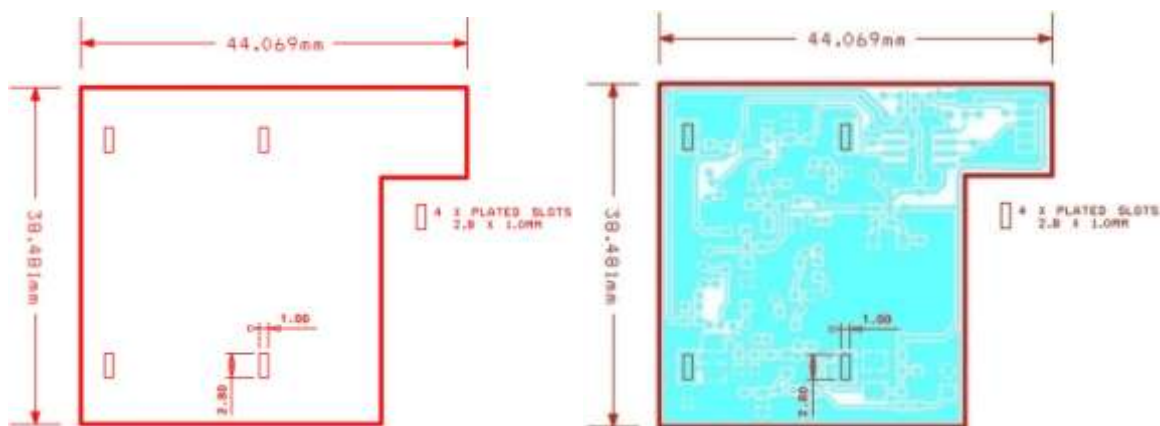
2. **Do not provide actual routing layers** for board contours or inside milling.

Routing data is production-specific depending on the rout tools, tool compensations, routing order and direction used by each PCB fabricator. This means that we cannot use customer-provided routing layers. We need to completely rework them, which can lead to confusion and misinterpretations which may result in incorrect boards.

It is our job as board producers to prepare correct production routing layers based on the information in your mechanical layer

3. A mechanical layer should **MINIMALLY contain:**

- The exact board outlines, ideally including dimensions (mm or inch).
- Exact positions and sizes for all inside milling, slots or cutouts, ideally including dimensions (mm or inch).



Outlines are best shown using a small line - e.g. 0.50mm (20mil) wide - where the center of the line represents the exact board outline.

IMPORTANT:

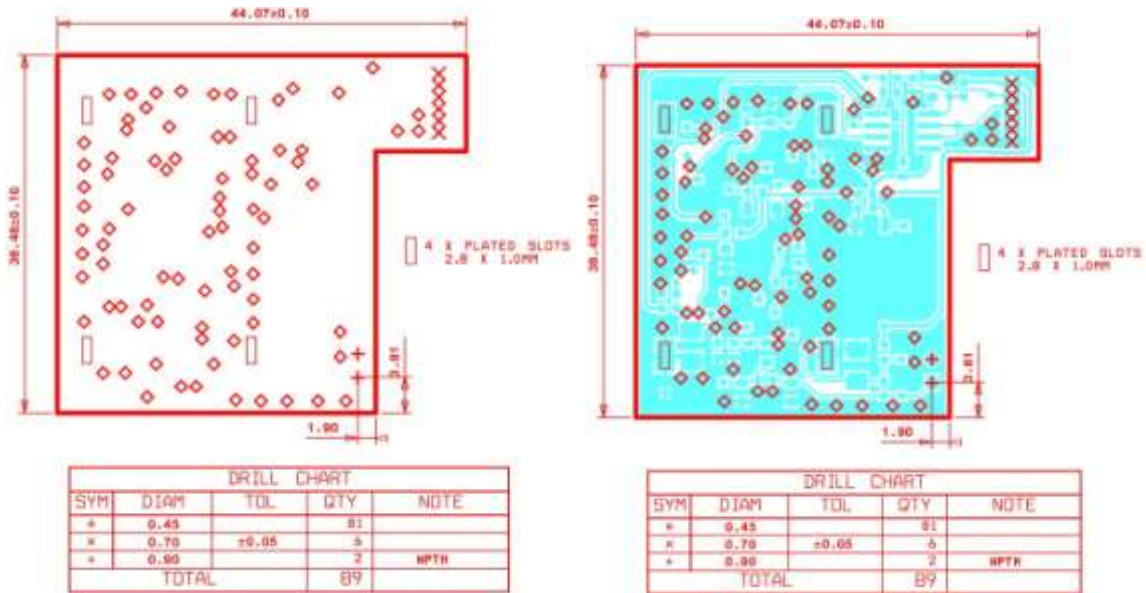
When no dimensions are given we will always take the center of the contour lines to be the exact outline of the board, regardless of their thickness.

4. Additional information that **should be included** in the mechanical plan **when needed:**

- A **reference hole**: the distance from one drill hole in X and Y to the PCB outline. This is particularly important when you only have NPTH holes without copper pads.
- Positional indication of all drills using symbols (=drill map). Use different symbols for each different drill size.
- **PTH/NPTH indication** for holes and slots
- If you supply panelized data include proper indications for break-routing and/or scoring (V-cut)
- A clear **layer sequence or buildup drawing** including all copper layers, soldermask and legend layers, any additional layers like peel-off or carbon, in the correct sequence viewed from top to bottom and with the correct corresponding data file name.

non-poolable option:

- **Special build-up:** If the build of your PCB requires material thicknesses, copper thicknesses or multilayer buildups which are different from our standard values then add this information to the layer sequence or buildup drawing.

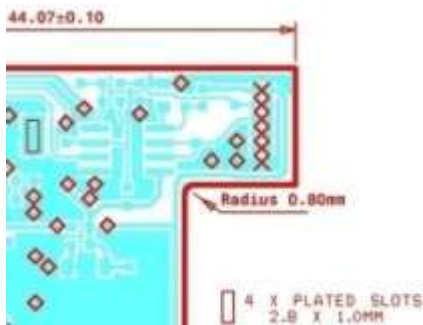


IMPORTANT:

We **ONLY** use a drill map to cross-check the Excellon drill file(s) for correctness. A drill map will NEVER be used to generate a drill file as this gives too many opportunities for error.

- The standard tool size used for all outline routing is 2.00mm (79mil).

This means that the standard minimum radius for inside corners is 1.00mm (39.5mil).



Requirements for a smaller radius on inner corners should be clearly indicated in the mechanical layer.

DESIGN TIP:

A sharp or 90 degrees inner corner can be obtained by placing a properly sized NPTH drill exactly on the board outline center of the inner corner or by a clever design of your board outline.



- The smallest width for any routed slot is 0.50mm (20mil) ENDSIZE.

7. Standard mechanical tolerances.

Routed boards

Tolerance on contour dimensions	+/- 0.20mm (+/- 8mil)
Tolerance on position of contour/cutouts to holes	+/- 0.20mm (+/- 8mil)
Tolerance on slot dimensions	
Width	+/-0.10mm (+/- 4mil)
Length	+/-0.20mm (+/- 8mil)

Scored (V-cut) boards

Tolerance on contour dimensions (after board separation)	+/- 0.30mm (+/- 12mil)
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When no tolerances are specified in your data, we will produce according to our standard tolerance specifications.

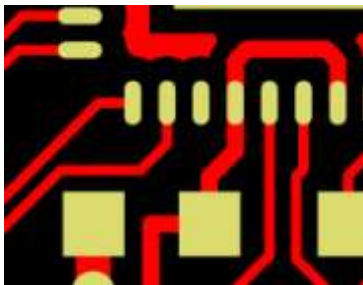
If you require tighter tolerances these should be clearly indicated in the mechanical layer and tool list. They will increase the cost of the PCB so should not be used without a compelling reason.

Soldermask

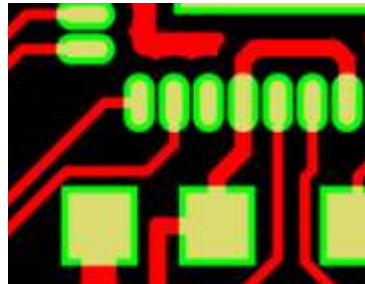
- When generating output data for soldermask, **there is no need to oversize or compensate the soldermask pads.**

It is better to leave the soldermask pads at the same size as the copper pads. We will then set the soldermask to suit the technological needs for proper production and assembly of the boards.

Preferred version without oversizing

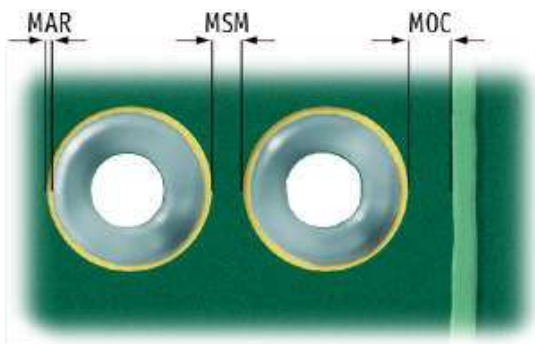


Less good: pads are oversized



- Soldermask preparation rules that we use:**

We set the values for soldermask preparation according to the PCB pattern class. The different features are shown in the diagram:



MAR (Mask Annular Ring) – the clearance between the soldermask and the copper pad

MSM (Mask Segment) – the bridge of soldermask between adjacent pads

MOC (Mask Overlap Clearance) – the soldermask cover between a track or plane and an adjacent soldermask window

We always start by applying the standard values to the complete soldermask. Depending on the design we can reduce these standard values at particular places down to the minimum accepted values to generate the best soldermask.

The standard value for MAR, MSM and MOC is 0.1000mm (4mil) for all pattern classifications.

The **MINIMUM accepted** values for MAR, MSM and MOC depend on the pattern classification according to the following table (values only in mm)

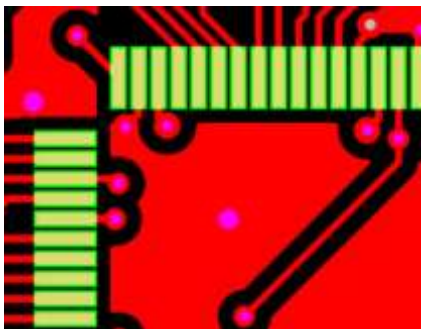
	MAR Mask Annular Ring	MSM Mask Segment	MOC Mask Overlap Clearance
Standard Value	0.1000	0.1000	0.1000
Minimum accepted values depending on Pattern Classification			
Pattern Classification	MAR Mask Annular Ring	MSM Mask Segment	MOC Mask Overlap Clearance
3	0.0600	0.1000	0.1000
4	0.0600	0.1000	0.1000
5	0.0600	0.1000	0.1000
6	0.0600	0.0800	0.0750
7	0.0600	0.0800	0.0625
8	0.0500	0.0800	0.0500
9	0.0400	0.0800	0.0500
10	---	---	---
(All values in mm)	!!!! → MOC takes precedence over MAR ← !!!!		

Important notice:

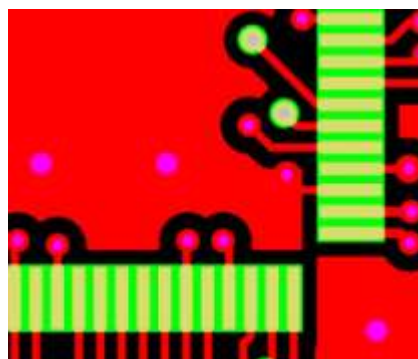
Value	→ These are safe values for production
Value	→ These values are on the limit of technology, so try to avoid them if possible.

IMPORTANT:

- Mask Segments smaller than 0.0800mm (3.15mil) will be removed.



→ This will be converted to the image below if the Mask Segment (MSM) between the pads is less than 0.0800mm (3.15mil)



- For **NPTH drills without copper pad** the **Mask Annular Ring (MAR)** is **ALWAYS 0.125mm** (4.92mil) independent of the pattern class.

3. **Tented vias: the copper pad of the via is covered with soldermask.**

IMPORTANT: If you require tented vias please make sure that you generate your soldermask data without soldermask pads for vias.

Tented via technology DOES NOT automatically mean that the via hole is fully closed or covered with soldermask. The maximum via ENDSIZE that can be closed with soldermask is 0.25mm (10mil). Completely closed via holes can only be guaranteed using ViaFill (See section ViaFill)

4. NPTH holes without copper pad should ALWAYS have a soldermask clearance pad.

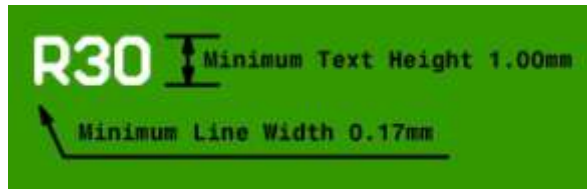
- When generating output include the board outline in your soldermask layers. This is best done using a small line - e.g. 0.50mm (20mil) wide - where the center of the line is the exact board outline. We will remove the line from the final production ready data.

IMPORTANT:

If you require board edge areas of your PCB to be free of soldermask, use a wide line to indicate the board outline. The line-width should be at least 2.00mm (79mil), resulting in 1.00mm (39.5mil) border free of soldermask. It is also advisable to indicate the soldermask-free border in the mechanical plan.

Legend Print

- Specifications for Legend Print:
 - Minimum Legend Line Width: 0.17mm (7mil)
 - Minimum Text height for good readability: 1.00mm (39.5mil).



- The Legend Print will **ALWAYS be broken – or clipped – against the corresponding soldermask layer.**

Clipping rules:

- Legend clipping clearance is 0.10mm (4mil). This means that we clip the legend 0.10mm (4mil) back from the soldermask openings.
- Any bits of line smaller than 0.17mm (7mil) are removed.



In absence of a soldermask layer, the legend print is clipped against the corresponding copper layer. If there is no copper layer, the legend is clipped against the drill layer.

DESIGN TIP:

To avoid your legend being clipped maintain a minimum distance of 0.20mm (8mil) between your legend elements and the copper image. This 0.20mm (8mil) = 0.10mm (4mil) Soldermask Annular Ring + 0.10mm (4mil) Legend Clipping Clearance.

- All legend text must be correctly readable.

As a **PCB is always viewed from top to bottom through the PCB**, text on the top layer of your board should be readable and text on the bottom layer should be non-readable or mirrored.
- Include the board outline in your legend layers output data.

This is best done using a small line - e.g. 0.50mm (20mil) wide - where the center of the line is the exact board outline. This line will be removed by us from your design.

In all cases we will clip away any legend text within 0.25mm (10mil) of the board edge.
- It is **NOT ADVISABLE** to place a legend layer on the copper layer side of a PCB without a soldermask layer.

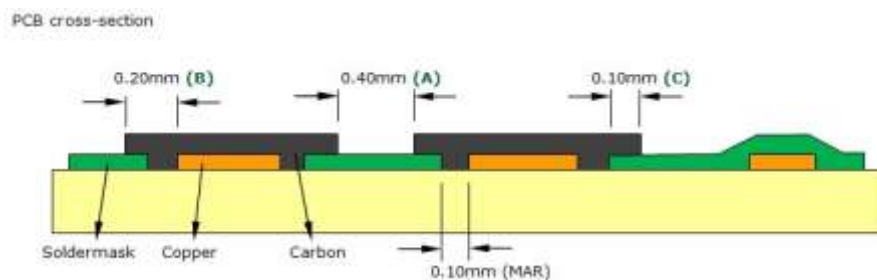
Carbon

1. Carbon elements or patterns are printed with a conductive carbon ink and can be used for keyboard contacts, LCD contacts, jumpers, etc...
2. Always clearly indicate on which side of the PCB carbon is to be applied. This can be on one side or on both sides.

IMPORTANT:

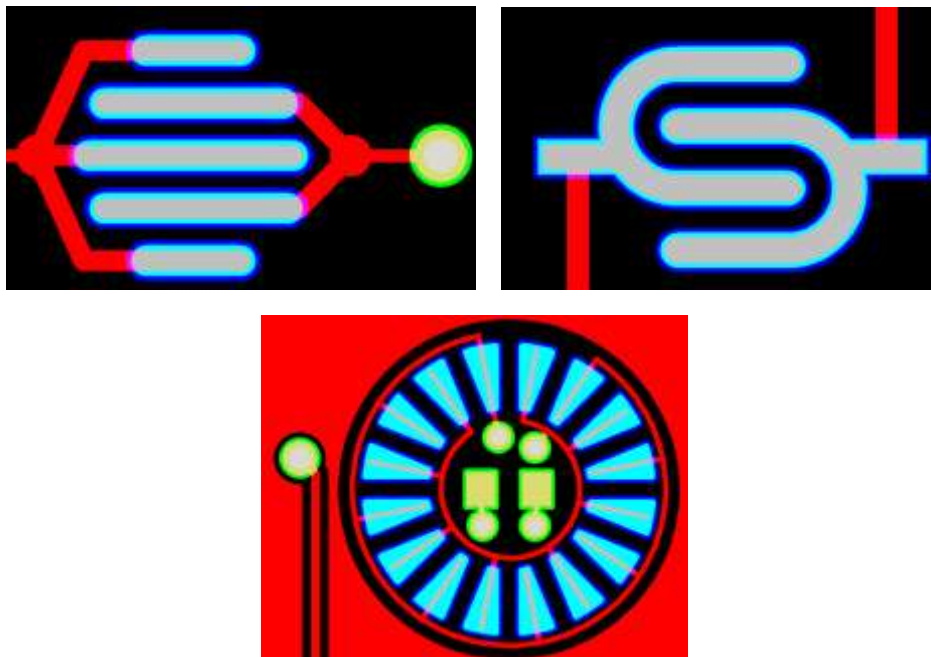
Indicate the position by proper file naming and a clear buildup or layer sequence description in the mechanical layer (See section Input data requirements – point 2, 3 and section Mechanical layer point 3)

3. When generating output include the board outline in your carbon layer(s). This is best done using a small line - e.g. 0.50mm (20mil) wide - where the center of the line is the exact board outline. We will remove this line from the production-ready data.
4. Overall carbon design rule specifications:



- Minimum carbon to carbon spacing **(A)**: 0.400mm (16mil)
- Minimum carbon line width: 0.300mm (12mil)
- Minimum carbon on copper overlap **(B)**: 0.200mm (8mil)
- Minimum carbon on soldermask overlap **(C)**: 0.100mm (4mil)

5. These rules mean that you must have a minimal isolation or spacing of 0.80mm (16mil) between the copper elements of a typical carbon finger contact.
6. Some examples of properly designed carbon contacts:



RED = copper, GREEN/LIGHT BLUE = soldermask opening, DARK BLUE = carbon

Peel-off mask

- Peel-off masks are used to:
 - Protect selected solder holes and pads against solder plugging during mass soldering.
 - Protect gold-plated contacts or carbon elements during mass soldering.
- Generally the peel-off mask **is applied ONLY to 1 side of the PCB**, usually the bottom side.

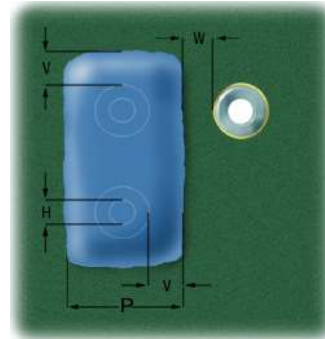
IMPORTANT:

If you require Peel-off on the top or bottom side of the PCB, please CLEARLY indicate this by means of proper file naming and clear buildup or layer sequence description in the mechanical layer (See section Input data requirements – point 2, 3 and section Mechanical layer point 3)

- When generating output include the board outline in your peel-off layer(s). This is best done using a small line - e.g. 0.50mm (20mil) wide - where the center of the line is the exact board outline. We will remove this line from the production ready data.
- Overall peel-off design rule specifications:

Minimum width of any Peel-off element (**P**): 0.500mm (20mil)
 Maximum coverable hole ENDSIZE (**H**): 6.00mm (236mil)
 Minimum overlap on copper pattern (**V**): 0.600mm (24mil)
 Minimum clearance to free copper (**W**): 0.600mm (24mil)

Minimum distance from PCB outline: 0.500mm (20mil)
 Tolerance on position: +/-0.300mm (12mil)

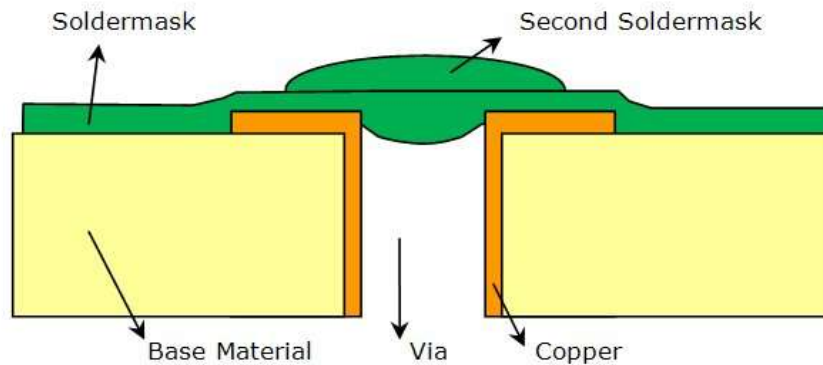


- Avoid using many different small peel-off areas randomly placed on your PCB.

Make the peel-off area as large as possible by connecting the separate peel-off areas wherever practical. This will make it easier to remove the peel-off after soldering.

ViaFill

1. Completely closed via holes can only be guaranteed by using ViaFill.
2. The maximum via hole ENDSIZE that can be completely closed is 0.25mm (10mil).
3. ViaFill is done by covering the via pad and via hole with a second layer of soldermask.



4. ViaFill data should be provided as a Gerber file containing only the via pads that need to be filled and the PCB board outline.
5. When generating output include the board outline in your ViaFill layer. This is best done using a small line - e.g. 0.50mm (20mil) wide - where the center of the line is the exact board outline. We will remove this line from the production ready data.
6. Typically ViaFill **is applied ONLY to 1 side of the PCB**. Which side is dependent on the board design.

IMPORTANT:

CLEARLY indicate on which side of the PCB (top or bottom) the ViaFill should be applied. Use proper file naming and clear buildup or layer sequence description in the mechanical layer (See section Input data requirements – point 2, 3 and section Mechanical layer point 3)

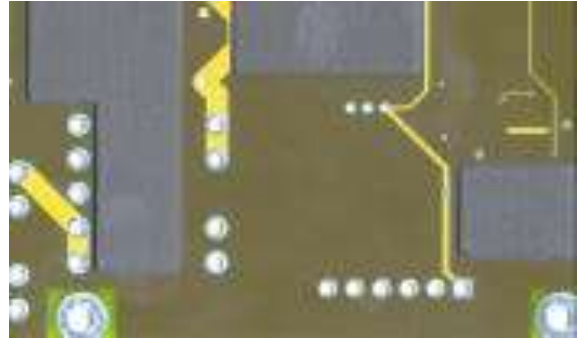
Heatsink paste

1. Heatsink paste is a paste that consists of a special polymer which is filled with finely dispersed solid particles. The polymer can easily be applied to a surface using screen or stencil printing and becomes fixed and functional after a drying or baking process.

The dispersed solid particles provide the thermal conductivity needed for the paste to act as a heatsink.

Heatsink paste can be used to create printed heatsinks of various geometric shapes directly on a PCB as an alternative to metal-foil heatsinks or externally fixed heatsinks.

Example of heatsinks created with heatsink paste:



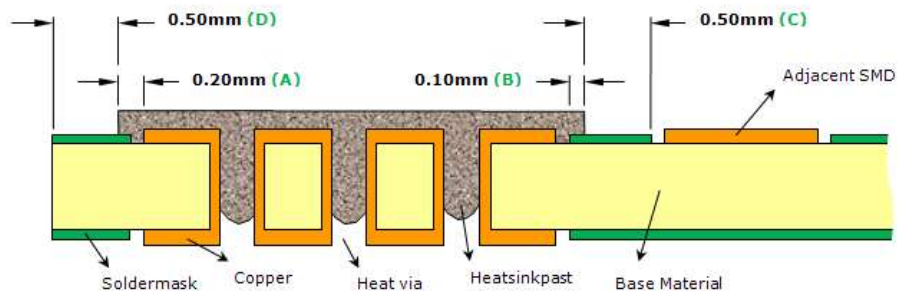
2. Always clearly indicate on which side of the PCB the heatsink paste is to be applied. This can be on one side or on both sides.

IMPORTANT:

Indicate the position by proper file naming and a clear buildup or layer sequence description in the mechanical layer (See section Input data requirements – point 2, 3 and section Mechanical layer point 3)

3. When generating output include the board outline in your heatsink paste layer(s). This is best done using a small line - e.g. 0.50mm (20mil) wide - where the center of the line is the exact board outline. We will remove this line from the production ready data.
4. Overall heatsink paste design rule specifications:

The area covered with heatsink paste must be **soldermask free**



- Minimum heatsink paste on copper overlap **(A)**: 0.20mm (8mil)
- Minimum heatsink paste on soldermask overlap **(B)**: 0.10mm (4mil)
- Minimum distance between heatsink paste and any adjacent soldermask opening **(C)**: 0.50mm (20mil)
- Minimum distance between heatsink paste and the PCB outline (incl. NPTH holes and slots) **(D)**: 0.50mm (20mil)
- Minimum heatsink paste line width: 0.30mm (12mil)

5. The recommended end size of the heat vias is between 0.80mm (32mil) and 1.20mm (48mil).
6. The recommended coating thickness of the heatsink paste is 100 μ (4mil) or 200 μ (8mil).
7. Heatsink paste is NOT compatible with Immersion Ag or Immersion Sn as plating finish.

Track Width Graphic

